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10/015,749	12/17/2001	Kazuhiro Sonoda	35.C16029	2844

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EXAMINER	
VILLECCO, JOHN M	
ART UNIT	**PAPER NUMBER**
2612	6

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,749	SONODA ET AL.	
	Examiner	Art Unit	
	John M. Villecco	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *4 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *N/A* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The USPTO is participating in a search exchange pilot program with the Japanese Patent Office (EPO). As part of the pilot program, the USPTO has received a copy of the Office Action prepared by the JPO on the counterpart JP application for which priority under 35 U.S.C. 119(a) is claimed. The references cited in the JPO Office Action have been considered by the examiner and have been listed on the PTO-892 form. A copy of these references is not being furnished to applicant with this Office action. It will not be necessary for applicant to submit these references in an information disclosure statement.

Claim Objections

2. **Claims 14 and 22 are objected to** because of the following informalities: In line 6 of claim 14, applicant recites the limitation of a "corrected double sampling circuit". This appears to be a translation error and that applicant meant to use the phrase – correlated double sampling circuit –. The same error can be found in line 6 of claim 22. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 6 and 8-23 are rejected under 35 U.S.C. 112, first paragraph**, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, in line 4 of claim 6 applicant states that the color filters are not integrated on the substrate. It is assumed from the disclosure that applicant is talking about Figure 14, in which the color filters (11) are not formed on the substrate (10). It is submitted that in this figure the color filters (11) are integrated on the substrate. Merriam-Webster's Collegiate Dictionary discloses integrated to mean: 1) to form, coordinate, or blend into a functioning or unified whole; or 2) to unite with something else. Based on the above description, it is clear that the color filters are "integrated" on the substrate since in combination they form parts of the package found in Figure 14. For examination purposes it will be assumed that the applicant means that the color filters are not formed directly on top of the substrate.

5. In line 5 of claims 8 and 16, applicant states that the lens is not integrated with the pixel area. Using the definition provided above, it is clear that the lens is integrated with the pixel area. For examination purposes it will be assumed that the applicant means that the lens not formed directly on the pixel area.

6. ***Claims 9-14 and 17-22 are rejected*** based upon their dependency upon claims 8 and 16, respectively.

7. Since ***claims 15 and 23*** include claims 8 and 16, it follows that they are also rejected.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. **Claims 11 and 19 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Regarding ***claims 11 and 19***, applicant recites both a substrate and a semiconductor substrate which are different from each other. A second substrate can be found nowhere in the specification. There is disclosure of a semiconductor substrate, but not a second substrate to which the semiconductor substrate in mounted. For examination purposes it will be assumed that applicant is trying to claim the mounting board (306) found on page 6, line 23.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Muramatsu (Japanese Publ. No. 2000-152085 A).

13. Regarding ***claim 1***, Muramatsu discloses an image pickup apparatus which is integrated on a substrate. More specifically, the apparatus includes a pixel area comprised of pixel blocks 22A, 22B, 22C and 22D wherein each of the pixel blocks is inherently comprised of a plurality of pixels. The pixel area is integrated on a substrate (24). Furthermore, as shown in Figures 8A and 8B, the center of the pixel area is and the center of the substrate (24) substantially coincide with each other. See paragraphs 0053-0057.

14. As for ***claim 2***, Muramatsu discloses that the substrate (24) includes processing circuits 23A1, 23A2, 23B1, 23B2, 23C1, 23C2, 23D1, 23D2 which are arranged to perform predetermined processing on the image signal. The processing circuits are arranged on each side of the pixel area. See Figure 8B.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Bohr (U.S. Patent No. 6,495,897).

17. Regarding ***claim 3,*** as mentioned above in the discussion of claim 1, Muramatsu discloses all of the limitations of the parent claim. Additionally, Muramatsu discloses that the substrate (24) includes processing circuits 23A1, 23A2, 23B1, 23B2, 23C1, 23C2, 23D1, 23D2 which are arranged to perform predetermined processing on the image signal. The processing circuits are arranged on each side of the pixel area. See Figure 8B. However, Muramatsu fails to specifically disclose a dummy circuit or pad located on the other side. While Muramatsu does disclose that processing circuits can be contained on one side of the pixel area, Muramatsu does not disclose a dummy circuit on the other side. Bohr, on the other hand, discloses that it is well known in the integrated circuit art to maintain a uniform density throughout the integrated circuit by implementing dummy areas in the open areas. As stated in column 1, lines 16-37, dummy

structures can be located throughout an integrated circuit to improve planarization during chemical mechanical polishing (CMP). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a dummy circuit on a side opposite of where a processing circuit is located in Muramatsu so that planarization is improved.

18. **Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Kochi et al. (U.S. Patent No. 6,188,094).**

19. Regarding ***claim 4***, as mentioned above in the discussion of claim 1, Muramatsu discloses all of the limitations of the parent claim. However, Muramatsu fails to specifically disclose that the substrate includes an area planarized by chemical mechanical polishing (CMP). Kochi, on the other, hand, discloses that it is well known in the art to perform chemical mechanical polishing on a substrate in order to level out the surface. See column 5, lines 13-17. This process is well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform CMP on the substrate of Muramatsu so that the top level of the substrate package is leveled off.

20. **Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Meyers (U.S. Patent No. 6,137,535).**

21. Regarding ***claim 5***, as mentioned above in the discussion of claim 1, Muramatsu discloses all of the limitations of the parent claim. Additionally, the pixel groups of Muramatsu are formed by a two-dimensional array of pixels. However, Muramatsu fails to specifically disclose lenses that correspond to the respective pixel groups to form light into images on the

pixel groups. Meyers, on the other hand, discloses a compact digital camera with segmented fields of view. More specifically, Meyers teaches an image sensor formed by subgroups of photodetectors (22). Each subgroup of photodetectors (22) has a lens (12) associated with it. See Figures 1a and 1b and column 4, lines 27-62. By forming lenses over the subgroups of photodetectors the impinging light is directed and focused onto the imaging element. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a lens for each of the pixel areas of Muramatsu so that light is directed and focused onto the face of the pixel areas.

22. **Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Meyers (U.S. Patent No. 6,137,535) and further in view of Park et al. (U.S. Patent No. 5,677,200)**.

23. Regarding ***claim 6***, as mentioned above in the discussion of claim 5, both Muramatsu and Meyers disclose all of the limitations of the parent claim. Additionally, Meyers discloses that each of the respective pixel groups comprises color filters. See Figure 1b and column 5, lines 40-50. However, neither Muramatsu nor Meyers specifically discloses that the color filters are not integrated on the substrate. Park, on the other hand, discloses that it is well known in the art to locate the color filter away from the substrate and not integrated with the substrate. (Please see the 112, 1st rejection above.) As shown in Figure 2, the substrate (20 is formed below the photodiode (21-n). Above the photodiode is a microlens with color filters (28-n) disposed over the microlens (26). See column 3, line 55 to column 4, line 14. This type of arrangement prevents color mixing and improves sensitivity (col. 2, lines 45-60. Therefore, it would have

been obvious to one of ordinary skill in the art at the time the invention was made to locate the color filters away from the substrate so that color mixing is prevent and sensitivity is improved.

24. **Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Hashimoto et al. (U.S. Patent No. 2000-152086 A)**.

25. Muramatsu discloses an image pickup apparatus which is integrated on a substrate. More specifically, the apparatus includes a pixel area comprised of pixel blocks 22A, 22B, 22C and 22D wherein each of the pixel blocks is inherently comprised of a plurality of pixels. The pixel area is integrated on a substrate (24). Furthermore, as shown in Figures 8A and 8B, the center of the pixel area is and the center of the substrate (24) substantially coincide with each other. See paragraphs 0053-0057.

However, Muramatsu fails to specifically disclose that the image pickup apparatus includes a signal processing circuit arranged to processing the signal from the image pickup apparatus or a memory. Hashimoto, on the other hand, discloses that it is well known in the art to include a signal processing circuit and a memory within an image pickup system. As shown in Figure 16, the image pickup apparatus includes a signal processing circuit (73) and a memory. See paragraph 0065. By including a signal processing circuit and memory, the image output from the sensor in Muramatsu can be turned into a meaningful image signal and can be stored for future use. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a signal processing circuit and a memory with the image pickup apparatus of Muramatsu.

26. **Claims 8-10 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Fujii (Japanese Publ. No. 11-330442)**.

27. Regarding ***claim 8***, Muramatsu discloses an image pickup apparatus which is integrated on a substrate. More specifically, the apparatus includes a pixel area comprised of pixel blocks 22A, 22B, 22C and 22D wherein each of the pixel blocks is inherently comprised of a plurality of pixels. The pixel area is integrated on a substrate (24). Furthermore, as shown in Figures 8A and 8B, the center of the pixel area is and the center of the substrate (24) substantially coincide with each other. See paragraphs 0053-0057. Muramatsu discloses that the substrate (24) includes processing circuits 23A1, 23A2, 23B1, 23B2, 23C1, 23C2, 23D1, 23D2 which are arranged to perform predetermined processing on the image signal. The processing circuits are arranged on each side of the pixel area. See Figure 8B.

However, Muramatsu fails to specifically disclose that the image pickup apparatus includes a lens arranged to form light into an image on the pixel area, wherein the lens is not integrated with the pixel area and that the substrate and the lens are united. (Please see the 112, 1st rejection above.) Fujii, on the other hand, teaches that it is well known in the art to form a lens over a pixel area. As shown in figure 3, Fujii discloses a lens (10) which includes glass (9) and forms light into an image on a pixel area on the image sensor (2). The lens is located away from the pixel area. Furthermore, when used in combination with Muramatsu the substrate and the lens of Fujii would be united. By forming a lens over the substrate light is focused onto the imaging element to thereby form a clear image. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to include a lens over the pixel area so that light is focused onto the pixel area and a clear image is formed.

28. As for ***claim 9***, as shown in Figure 3, Fujii discloses that the lens (10) is fixed on two sides on the periphery of the pixel area.

29. With regard to ***claim 10***, as shown in Figure 3, the lens of Fujii includes a glass (9) arranged above the pixel area and that the lens (10) is fixed to the glass.

30. Regarding ***claim 12***, Muramatsu discloses that the pixel areas (23A-D) are integrated on the substrate (24).

31. As for ***claim 13***, Muramatsu discloses that circuits 23A1, 23A2, 23B1, 23B2, 23C1, 23C2, 23D1, and 23D2 include address decoders and scanning circuits. See paragraph 0053.

32. With regard to ***claim 14***, discloses that the processing circuits include A/D converters on opposite sides of the pixel areas. See Figure 6 and paragraph 0043.

33. **Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Fujii (Japanese Publ. No. 11-330442) and further in view of Makino et al. (Japanese Publ. No. 11-150253)**.

34. Regarding claim 11, as mentioned above in the discussion of claim 8, both Muramatsu and Fujii disclose all of the limitations of the parent claim. However, neither of the aforementioned references specifically discloses that the pixel area is formed on a semiconductor substrate and that the semiconductor substrate is formed on the substrate. Makino, on the other hand discloses that it is well known in the art to combine substrates to form an image sensor. (See the 112, 2nd rejection above.) Makino discloses a semiconductor substrate (12) mounted to

a wiring board (18). By mounting the semiconductor substrate to a board, signals can be processed and output. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the semiconductor substrate to the wiring board so that it is connected to the outside and signals can be further processed and output.

35. **Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Fujii (Japanese Publ. No, 11-330442) and further in view of Hashimoto et al. (U.S. Patent No. 2000-152086 A).**

36. Claim 15 is considered substantively similar to claim 7. Please see the discussion of claim 7 above.

37. **Claims 16-18 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Fujii (Japanese Publ. No, 11-330442) and further in view of Bohr (U.S. Patent No. 6,495,897).**

38. ***Claim 16*** is considered substantively equivalent to claim 8 with the added limitation of a dummy circuit or pad arranged on the other of two sides. As mentioned above in the discussion of claim 1, Muramatsu discloses all of the limitations of the parent claim. Additionally, Muramatsu discloses that the substrate (24) includes processing circuits 23A1, 23A2, 23B1, 23B2, 23C1, 23C2, 23D1, 23D2 which are arranged to perform predetermined processing on the image signal. The processing circuits are arranged on each side of the pixel area. See Figure 8B. However, Muramatsu fails to specifically disclose a dummy circuit or pad located on the other side. While Muramatsu does disclose that processing circuits can be contained on one side of the

pixel area, Muramatsu does not disclose a dummy circuit on the other side. Bohr, on the other hand, discloses that it is well known in the integrated circuit art to maintain a uniform density throughout the integrated circuit by implementing dummy areas in the open areas. As stated in column 1, lines 16-37, dummy structures can be located throughout an integrated circuit to improve planarization during chemical mechanical polishing (CMP). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a dummy circuit on a side opposite of where a processing circuit is located in Muramatsu so that planarization is improved.

39. ***Claim 17*** is considered substantively equivalent to claim 9. Please see the discussion of claim 9 above.

40. ***Claim 18*** is considered substantively equivalent to claim 10. Please see the discussion of claim 10 above.

41. ***Claim 20*** is considered substantively equivalent to claim 12. Please see the discussion of claim 12 above.

42. ***Claim 21*** is considered substantively equivalent to claim 13. Please see the discussion of claim 13 above.

43. ***Claim 22*** is considered substantively equivalent to claim 14. Please see the discussion of claim 14 above.

44. **Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Fujii (Japanese Publ. No, 11-330442) and**

further in view of Bohr (U.S. Patent No. 6,495,897) and Makino et al. (Japanese Publ. No. 11-150253).

45. Regarding claim 19, as mentioned above in the discussion of claim 16, Muramatsu, Fujii, and Fujii disclose all of the limitations of the parent claim. However, none of the aforementioned references specifically discloses that the pixel area is formed on a semiconductor substrate and that the semiconductor substrate is formed on the substrate. Makino, on the other hand discloses that it is well known in the art to combine substrates to form an image sensor. (See the 112, 2nd rejection above.) Makino discloses a semiconductor substrate (12) mounted to a wiring board (18). By mounting the semiconductor substrate to a board, signals can be processed and output. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the semiconductor substrate to the wiring board so that it is connected to the outside and signals can be further processed and output.

46. **Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu (Japanese Publ. No. 2000-152085 A) in view of Fujii (Japanese Publ. No, 11-330442) and further in view of Bohr (U.S. Patent No. 6,495,897) and Hashimoto et al. (U.S. Patent No. 2000-152086 A)**.

47. Claim 23 is considered substantively similar to claim 7. Please see the discussion of claim 7 above.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (For either formal or informal communications intended for entry. For informal or draft communications, please label "**PROPOSED**" or "**DRAFT**")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (703) 305-1460. The examiner can normally be reached on Monday through Thursday from 7:00 am to 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service desk whose telephone number is (703) 306-0377.

JMV
9/8/03

WENDY R. GARBER
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